Ryan Zhang

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TECHNICAL SKILLS

| Back-End | Java (fluent), Python (fluent), Javascript, NodeJS, $C/C#$ |
|--------------------|---|
| Back-End Libraries | Pytesseract, PyTorch, OpenCV, Numpy, Flask, Processing, BS4 |
| Front-End | HTML, CSS, Bootstrap |
| Miscellaneous | SQL, VHDL, Photoshop, Premiere Pro, Excel, MATLAB |

SUMMARY

A 2nd Year Computer Systems Engineering undergraduate student at the University of Warwick, with extensive full-stack experience. Interested in hardware and full stack software, with a particular focus on FPGA/CPU development in VHDL and applications of AI. Have experience in web and game development. Adaptable, curious, socially adept and a great team player. Looking for a challenging position to introduce me to industry, and grow and learn from an experienced team.

EDUCATION

| 2016 - 2018 | KS3 at Skinners' School |
|----------------|---|
| 2018 - 2023 | GCSE & A-Level at Tonbridge School |
| | A-Levels: Mathematics (A [*]), Further Mathematics (A), Computer Science (A), Religious Studies (A) |
| | 9 GCSE's grade 9 including Mathematics, Computer Science and English Language |
| | Involved in: School Council, Anti-Bullying Council, Online Safety Council, Learning Mentor |
| | Program, Debate Team, Programming Club, CANSAT Team |
| 2023 - Present | BEng Computer Systems Engineering at University of Warwick |
| | Achieved 2:1 during First Year |
| | Taking Algorithms CS260 and Semiconductor Materials and Devices ES2D6 as optional |
| | modules during Second Year |
| | Involved in: Student Union Societies Forum Member, President of Culture Society, President |
| | of Travel Society, Debate Coordinator at Discourse Society |

WORK EXPERIENCE

Website Volunteer at St Philips Church

- Responsible for regular upkeep of WordPress site such as designing and updating of event banners in Photoshop.
- Researched and implemented SEO to boost site visibility.
- Developed a "sermons" subdomain with all sermon recordings.

Tech Consultant at Offer Page

- Performed legal and practical feasibility tests of scraping reed.co.uk to generate job market reports for a given job title.
- Researched deploying scraper script on an Amazon Elastic Container Service, using Docker.
- Regularly communicated with client for program specifications.
- Developed a Python prototype with Selenium to summarise reed.co.uk listings using LLMs and regex.

August 2018 - April 2019

October 2023 - December 2023

Projects

Civilization 5 Remake (Java) with LLM-Based AI

- Independently developed a remake of the real-time strategy video game using the Processing GUI Library.
- Integrated world generation, local multiplayer, a combat system, multiple victory conditions, and a scaled-down technology tree.
- Developed a Llama 70B-based CPU to interpret and act on game states with a multi-agent architecture.

Playing Flappy Bird with a Deep Neural Network (Python)

- Developed a remake of Flappy Bird using PyGame, using PyTorch to develop the neural network.
- Learned state-space discretization and RL exploration strategies.

FPGA Projects (Verilog + Vivado Design Software)

- Stystolic-array matrix multiplier
- Hamming code (7,4) error detection and correction
- Basic calculator

Wrote Research Paper on the Future of CPUs

- Focused on heterogeneous architectures, neural networks in branch prediction, and case studies on AMD's 3D V-Cache and Intel's Foveros.
- Performed market research on optical, quantum and distributed-edge computing.

EVENTS & WORKSHOPS

| 2019 & 2020 | Perse Coding Team Challenge |
|--------------|---|
| | Chosen to represent Tonbridge both years in a national two-person team competitive pro- |
| | gramming competition. |
| 2019 & 2020 | English Speaking Union |
| | Public speaking captain for both years, led Tonbridge to the South-East regional final in 2020. |
| January 2024 | Warwick Model United Nations |
| | Represented China in a simulated United Nations conference, researched and debated issues |
| | on the implications of technology, particularly AI ethics. |
| April 2024 | Intel FPGA Technical Training Programs |
| | Completed the "Beginner Intel FPGA Designer" course, attended Verilog HDL Basics and |
| | Verilog HDL Advanced instructor-led webinars offered by Intel. Supplemented learning with |
| | other online resources. |

References and Cover Letter available upon request. More details @ ryan-zhang.com